This Page Is Inserted by IFW Operations and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents will not correct images, please do not report the images to the Image Problem Mailbox.

FEB 1 2 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First-Named Inventor: RUTTEN, Ivo

Application No.: 10/005,974 Conf.: 2642

Date Filed:

11/08/2001

Notice of Allowance Date:

Docket No.: US01 8179

Art Unit:

2829

Examiner:

Pert, Evan T.

Title: Preconditioning Integrated Circuit for Integrated Circuit Testing

Mail Stop Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 Facsimile: (703) 746-4000

CERTIFICATE OF TRANSMISSION under 37 CFR §1.8

I hereby certify that this correspondence is being facsimile transmitted to the United States and Trademark Office at facsimile number (703) 746-4000, on February 12, 2004 . The documents listed below are included in this transmission:

- ✓ Issue Fee Transmittal ALL required fees paid by deposit account
- ✓ Letter to Official Draftsman

✓ Three (3) sheets of Formal Drawings

(Signature)

Daniel L. Michalek

(Typed or printed name of person signing Certificate)

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION

Intellectual Property & Standards 1109 McKay Drive, M/S-41SJ

San Jose, California 95131

Telephone: (408) 474-9073

Facsimile: (408) 474-9082



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First-Named Inventor: RUTTEN, Ivo

Docket No.:

US01 8179

Application No.: 10/005,974 Conf.: 2642

Art Unit:

2829

Date Filed:

11/08/2001

Examiner:

Pert, Evan T.

Notice of Allowance Date: 11/12/2003

Customer No.: 24738

Title: PRECONDITIONING INTEGRATED CIRCUIT FOR INTEGRATED CIRCUIT

TESTING

Box ISSUE FEE Assistant Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

LETTER TO OFFICIAL DRAFTSMAN

Sir:

Enclosed please find three (3) sheets of corrected/substitute drawings for entry in the above-referenced patent application.

Please charge any fees which may be required, except the issue fee, or credit any overpayment to Deposit Account No. 14-1270.

Date:

Respectfully submitted,

Michael J. Ure Reg. No. 33,089

(408) 474-9077

Philips Electronics North America Corp.

1109 McKay Drive MS-41SJ San Jose, California 95131

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that on the date indicated below this correspondence is being faxed to or deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to "Commissioner for Paterts, P.O. Box 1450, Alexandria. VA 22313-1450".

(Signature) (Name)

Daniel L Michalek